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An Ultra Low power and High Performance of CMOS (6H-SiC) Current Mirrors in BSIM3v3 130nm Technology

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Abstract: *It has long been known that silicon carbide technology is used in high power and high temperature fields; this has made it an appropriate alternative to silicon technology in some electronic applications; and as the current mirror is considered the basic unit in designs analog integrated circuits. We have studied and compared basic current mirrors in 130nm CMOS(6H-SiC) technology using BSIM3v3 model in this article. To realize this work, we have used PSpice to study the output characteristic $I_{OUT}=f(V_{OUT})$, transfer characteristic $I_{OUT}=f(I_{IN})$ and variation of the output resistance as a function of temperature $R_{OUT}=f(T)$ in the range -200°C to 700°C with a supply voltage of 1.2V for these mirrors. As a result, we proposed the Multi-Stage mirror with n number of stages to improve the different characteristics of current mirror. The simulation results proved that, in addition to the good performance of our current mirrors compared to other research, they work well in low voltage less than 1V, ultra low power in the order of hundreds nW and ultra high output resistance is more than GΩ. Besides, these properties were characterized by a good current mirroring accuracy, which is represented in the current ratio (I_{OUT}/I_{IN}) that is equal to 1.*

Keyword: *6H-SiC, 130nm Technology, BSIM3v3 Model, Current mirror, Low power.*

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1. INTRODUCTION

Current mirror (CM) have been used for decades in operational amplifier [1], mixed-signal [2] and analog circuits [3], becoming one of the most important building blocks in designs analog integrated circuits [4].

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In this circuit, the input current, I_{IN}, is mirrored to the output branch, keeping its current, I_{OUT}, constant. In the ideal state of CM, the relation between the output and the input current (I_{OUT}/I_{IN}) should be independent of the temperature, such that the output current does not depend on the output voltage [5]. The current mirror performs both biasing and processing functions and works on copying an accurately-defined reference current in other circuit branches. For the high performance of a current mirror, this circuit must be designed with low input resistance (R_{IN}) and very high output resistance (R_{OUT}). The considered as the low supply voltage in present CMOS technologies, low input and low output operation voltages are fundamental requirements for the current mirror circuit [2].

In 2013, Michelly made a comparison between the performance of current mirrors (Common-source, Cascode and Wilson current mirrors architectures) in low temperature (150 K) with FD SOI nMOSFETs Silicon 2µm technology [5]. In 2016, Bhawna Aggarwal made the same comparison between basic current mirrors, but in 0.18 µm CMOS and BSIM3 technology [1].

What is perceptible in these researches is that they were limited to the study of mirrors using the silicon technique, and in order to study these current mirrors in low power we proposed new structures.

Silicon carbide (SiC) has been used instead of silicon (Si) for current mirror circuits manufacturing, due to its better physical properties than silicon (Si). It has a high breakdown field, a high saturation velocity of electrons and a high thermal conductivity [6], and has the potential to overcome the limitations imposed by power devices made of Si base material [7-8-9]. These CMs in SiC technology was characterized by high current, high voltage, high power and high temperature [10-11].

We have shown that the MOS transistors in Silicon Carbide (SiC) submicron (130nm) technology work well in low voltage and low power [12-13], for this we will use these transistors to increase the performance of current mirrors.

In this work, we will study the different basic current mirror circuits simple, cascode, wilson and widlar that based on use the MOS(6H-SiC) transistors with BSIM3v3 model in the first section. To carry out this study, we will simulate the different characteristics of our circuits output characteristic $I_{OUT}=f(V_{OUT})$, transfer characteristic $I_{OUT}=f(I_{IN})$ and variation of the output resistance as a function of temperature $R_{OUT}=f(T)$. For improved these characteristics, we will propose a new topology that is based on the cascode mirror in the second section of our work. This circuit is Multi-Stage of the *n* number of stages. Our work will be carried for 130nm technology, a supply voltage of 1.2V and temperatures between -200°C and 700°C, and we will use the OrCAD (PSpice) 16.5 software to simulate the different current mirror circuits.

2. THEORY OF MOS BASIC CMs

The principle of the basic current mirror is based on producing a copy of a current (reference current) in the output terminal of one active device (M2 in Figure 1 (a)) by controlling the current in another active device (M1 in Figure 1 (a)) [14]. Figure 1 shows the different current mirror circuits in MOS technology. Figure 1 (a) shows a simple current mirror SCM circuit with two MOS transistors M1 and M2. The drain of transistor M1 is shorted to its gate, so that it is operating in saturation region. In order for the current mirror to work properly, M2 must also be in saturation [15]. The drain currents can be expressed in this region as:

$$I_{REF}=\frac{1}{2}K_n'\left(\frac{W}{L}\right)_1(V_{GS}-V_T)^2(1+\lambda V_{DS1}) \quad (1)$$

$$I_{OUT}=\frac{1}{2}K_n'\left(\frac{W}{L}\right)_2(V_{GS}-V_T)^2(1+\lambda V_{DS2}) \quad (2)$$

Where W and L are the width and length of channel MOS transistor respectively, and $K_n'=\mu C_{ox}\frac{W}{L}$. μ is the mobility of the charge carriers of transistor, C_{ox} is the capacitance per unit area, λ is the channel length modulation parameter and V_T is the threshold voltage of transistor.

The mirror ratio MR is given by:

$$MR=\frac{I_{OUT}}{I_{REF}}=\frac{(W/L)_2}{(W/L)_1}\frac{(1+\lambda V_{DS2})}{(1+\lambda V_{DS1})} \quad (3)$$

For this work, the geometrical channel ratio (W/L) is constant for all MOSiC(6H-SiC) transistors. It is given:

$$\frac{I_{OUT}}{I_{REF}}=\frac{(1+\lambda V_{DS2})}{(1+\lambda V_{DS1})} \quad (4)$$

To determine the output resistance of a current mirror, the small-signal analysis of this CM [05-16] must be considered. The R_{OUT} of simple current mirror is given as:

$$R_{OUT}=r_{OUT2}=\frac{1}{g_{m2}}=\frac{1}{\lambda_2 I_{D2}} \quad (5)$$

Where r_{OUT2}, g_{m2} and λ_2 are the output resistance, transconductance and channel length modulation respectively of M_2. The simple current mirror problem is that the effect of channel length modulation was neglected for designing the current mirror [15].

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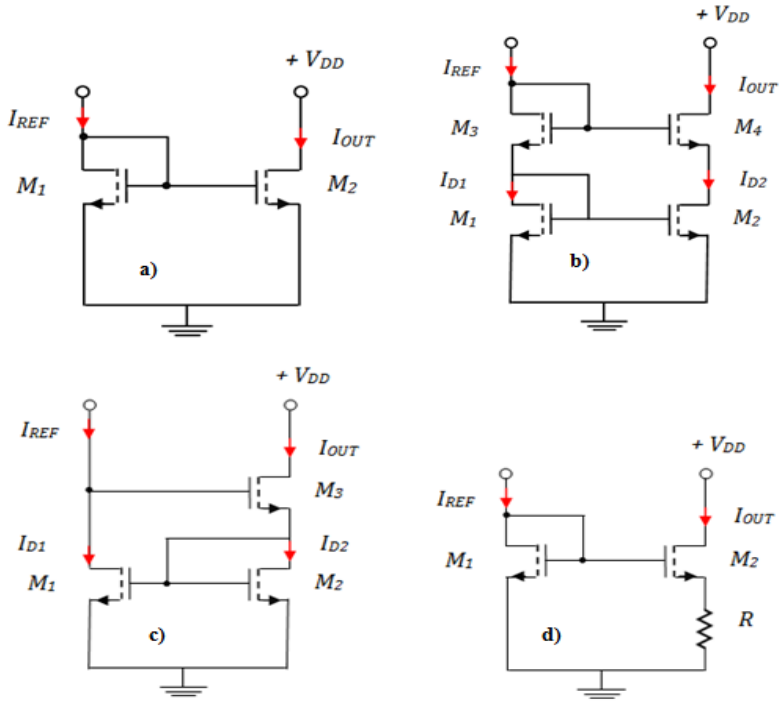

Figure 1 Basic current mirror circuits. a) Simple current mirror SCM, b) Cascode current mirror CCM, c) Wilson current mirror WilsonCM, d) Widlar current mirror WidlarCM.

To find the cascode current mirror we connected two simple mirrors as shown in Figure 1 (b). The actual ratio of this current mirror is given by:

$$\frac{I_{OUT}}{I_{REF}} = \frac{(W/L)_4}{(W/L)_1}\frac{(1+\lambda V_{DS4})}{(1+\lambda V_{DS1})} \quad (6)$$

The relation of output resistance for this mirror is given as follows [15]:

$$R_{OUT} = r_{OUT4}(1 + g_{m4}r_{OUT2}) + r_{OUT2} \quad (7)$$

To improve the performance characteristics of a simple CM, new architectures were proposed including the Wilson circuit (Figure 1 (c)) was proposed by Wilson [17]. In this mirror type the MR is given by (Equation 8), if the transistors all have the same geometric ratios.

$$\frac{I_{OUT}}{I_{REF}} = \frac{1+\lambda V_{GS}}{1+2\lambda V_{GS}} \quad (8)$$

The R_{OUT} output resistance of WilsonCM circuit is given as [01]:

$$R_{OUT} \approx \frac{g_{m1}r_{OUT1}g_{m3}r_{OUT3}}{g_{m2}} \quad (9)$$

Figure 1 (d) is the MOS version of the Widlar current mirror. In this circuit, the difference between the gate-source voltages of transistors M1 and M2 appears across resistor R, and output current I_{OUT} can be expressed as [16].

$$I_{OUT} = \frac{V_{GS1} - V_{GS2}}{R} = \frac{\sqrt{\frac{2I_{REF}}{K_{n1}}} - \sqrt{\frac{2I_{OUT}}{K_{n2}}}}{R} \quad (10)$$

Or

$$I_{OUT} = \frac{1}{R}\sqrt{\frac{2I_{REF}}{K_{n1}}}\left(1 - \sqrt{\frac{I_{OUT}}{I_{REF}}\frac{(W/L)_1}{(W/L)_2}}\right) \quad (11)$$

The mirror ratio MR for this mirror is given by:

$$\frac{I_{OUT}}{I_{REF}} = \frac{1}{R}\sqrt{\frac{2}{K_{n1}I_{REF}}}\left(1 - \sqrt{\frac{I_{OUT}}{I_{REF}}\frac{(W/L)_1}{(W/L)_2}}\right) \quad (12)$$

The output resistance of WidlarCM is higher than the one for the SCM, and is given as [16]:

$$R_{OUT} = r_{OUT2}(1 + g_{m2}R) \quad (13)$$

3. RESULTS AND DISCUSSION

3.1 MOS(6H-SiC) basic current mirrors

In this section, we provide simulation DC from a different basic current mirror of Figure 1 with 130nm

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CMOS (6H-SiC) technology. Figure 2 shows the output characteristic of our current mirrors I_{OUT} as a function of V_{OUT} for output voltage ranging from 0V to 1.2 V.

The variation of output current I_{OUT} is evaluated in the saturation mode for variations output voltage V_{OUT} in the ranges 0.4V, 0.15V, 0.35 and 0.3V for SCM, CCM, WilsonCM and WidlarCM respectively.

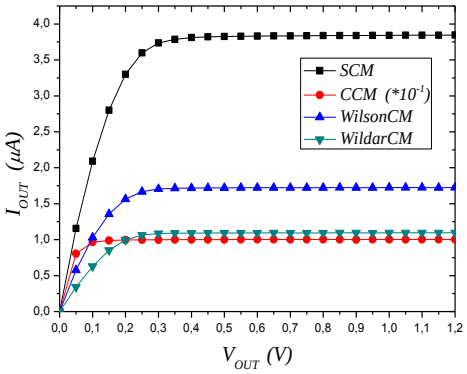
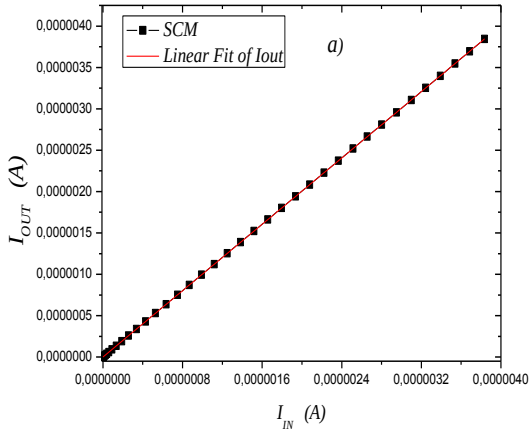
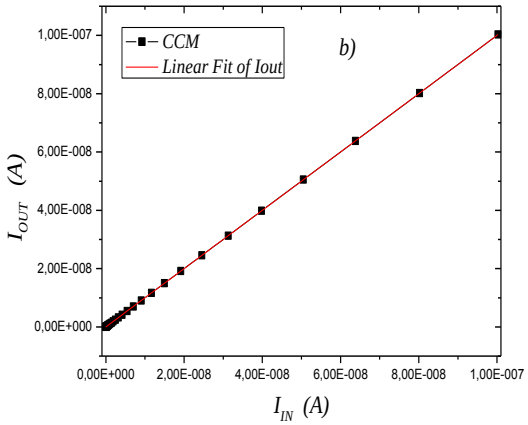
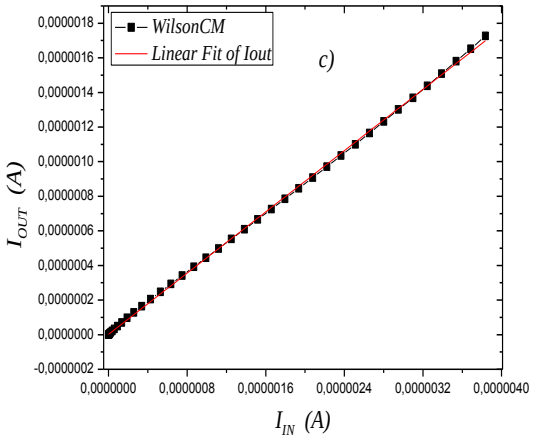


Figure 2. Output characteristic $I_{OUT}=f(V_{OUT})$ of basic MOS(6H-SiC) current mirrors.







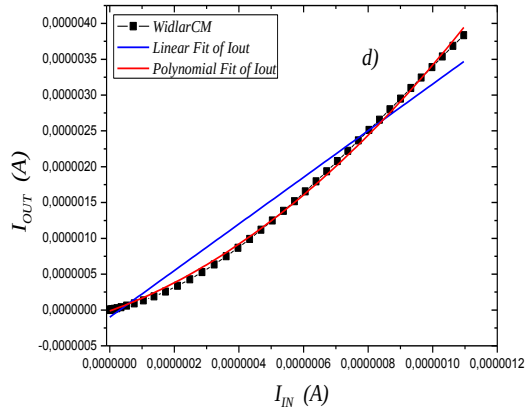


Figure 3 Transfer characteristic of basic current mirrors, a) SCM, b) CCM, c) WilsonCM, d) WidlarCM.

This characteristic shown that the cascode current mirror CCM is characterized by a low voltage and very low power compared to other types of the mirror, and the output current in this circuit is more stable whatever the variation of the output voltage this is consistent with literature [18-19]. These results, show that basic current mirrors in 130nm CMOS(6H-SiC) technology is working properly in a low voltage and characterized by a low power.

The current transfer characteristics are a very important characteristic in the current mirror to find the I_{OUT}/I_{IN} ratio. To find this characteristic, we have applied a voltage V_{OUT} = 1.2 V, and we varied the I_{IN} input current from 0A to 4µA of different current mirrors. The results of our simulation are presented in Figure 3.

Figure 3 shows the transfer characteristic I_{OUT} as a function of I_{IN} of the basic current mirror at room temperature. The output current I_{OUT} is linearly evolving as a function of the input current I_{IN} for the different basic current mirrors (Figure 3. a ,b and c), but the

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evolution of this characteristic for the WidlarCM is quasi-linear of a 1.60052 slope (Figure 3. d). The ratio (I_{OUT}/I_{IN}) values are 1.00237, 1 and 0.44236 for SCM, CCM and WilsonCM respectively. This characteristic show that the cascode current mirror CCM is characterized by the good current mirroring accuracy compared to other basic mirrors, and this is compatible with works in literatures as shown in Table I.
These characteristics showed that the electronic behavior of current mirrors in 130nm CMOS(6H-SiC) technology compatible with what is contained in the literature for CMs.

In order to identify the high performance of the current mirror, output resistance R_{OUT} must be studied, this resistance is found through the following relation [20]:

$$R_{OUT} = \frac{\delta V_{OUT}}{\delta I_{OUT}} \quad (14)$$

Figure 4 shows the evolution of the output resistance R_{OUT} as a function of temperature in the range of -200°C to 700°C for our current mirrors at supply voltage V_{DD}=1.2V.

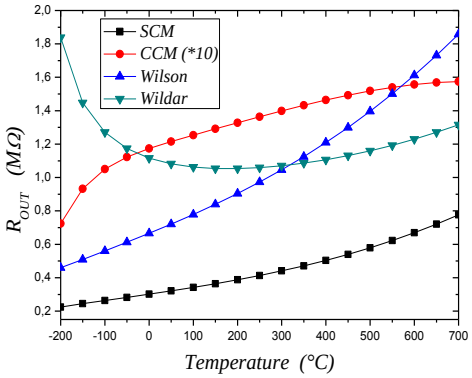

Figure 4 Output resistances as a function of temperature.

The output resistance R_{OUT} is slightly increased when the temperature increases for the basic current mirrors as shown in the figure. This evolution showed that the current mirror which is characterized by a high output resistance value is the CCM. The simulation results show that the output resistance of the different basic current mirror circuits in 130nm CMOS(6H-SiC) technology is very high of the order of MΩ at a very wide temperature range. To evaluation performance of our mirrors. In Table I, the comparison between our current mirrors in 130nm CMOS(6H-SiC) technology and some works on the basic CMs.

This section of our work showed that the basic CMs in 130nm CMOS(6H-SiC) technology works well in low voltage, low power and high temperature. And it has a high performance compared to those in presented in the literature, and in particular the cascode current mirror CCM circuit.

To improve the properties of basic current mirrors, we propose an architecture which is called multi cascade mirror MCCM.

3.2 Multi-Stage mirror

Figure 5 shows the Multi-Stage Current Mirror (MSCM) circuit. This mirror contains *n* number of stages one above the other as shown in this figure. In this work the *n* number of stages varies between 1 and 6 stage.

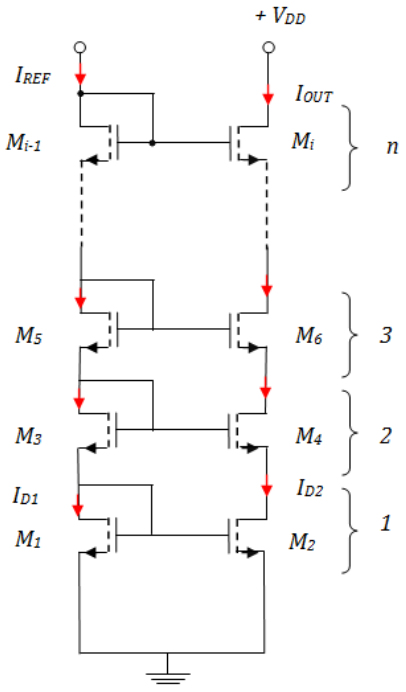

Figure 5 Multi-Stage Current Mirror circuit (MSCM).

TABLE I COMPARISON BETWEEN BASIC CMS IN MOS(6H-SIC) AND OTHER WORKS AT ROOM TEMPERATURE

CMs / Parameters	MOS BSIM3 180nm CMs [01]			MOS 250nm CMs [21]			MOS 350nm CMs [22]			MOS(6H-SiC) BSIM3v3 130nm CMs (This work)			
	SCM	CCM	WilsonCM	SCM	CCM	WilsonCM	SCM	CCM	WilsonCM	SCM	CCM	WilsonCM	WidlarCM
V_{DD} (V)	1.8	1.8	1.8	2.5	2.5	2.5	3.5	3.5	3.5	1.2	1.2	1.2	1.2
V_{min} (V)	0.1–0.4	0.5–0.9	0.5–0.9	0.7	1.4	1.94	0.5	0.88	0.55	0.4	0.15	0.35	0.3
Power Consumption	33.12 µW	28.69 µW	25.12 µW	6.25 mW	6.756 mW	6.849 mW	1.9 mW	2.15 mW	1.93 mW	1.5384 µW	15.053 nW	603.85 nW	328.69 nW
R_{OUT}	200 kΩ	14 MΩ	18 MΩ	47.34 KΩ	1.622 MΩ	1.71 MΩ	104.5 kΩ	1.120 GΩ	8.97 GΩ	312.01 kΩ	12 MΩ	695.53 kΩ	1.0953 MΩ
Ratio	1.066	1	0.925	1.093	1.0045	1.0045	0.995	1	1	1.00237	1	0.44236	1.60052

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According to the output characteristic of MSCM circuit, the results are summed up in Figure 6. This figure shows the evolution of the minimum output voltage V_{OUTmin} as a function of *n* number of stages at V_{DD}=1.2V and in room temperature.

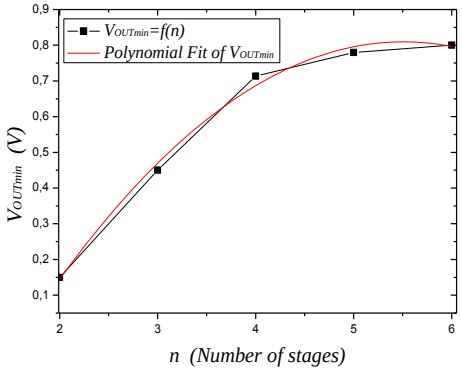

Figure 6 Minimum output voltage as a function of n for MSCM.

The increase of *n* number of stages in the Multi-Stage mirror has led to the decrease of the stabilization in the case of the low output voltage. For this, the minimum output voltage increases when the number of stages increases as shown in Figure 6. According to this simulation, the variation of the minimum output voltage V_{OUTmin} as a function of *n* number of stages is given by the following polynomial increasing relation:

$$V_{OUTmin} = -0.05403\ n^2 + 0.59522\ n - 0.82967 \quad (15)$$

The output current is decreased in the saturation regime when the number of stages is increasing at V_{DD}=1.2 V. This decrease in the current is necessarily led to decrease the power consumption as shown in Figure 7.

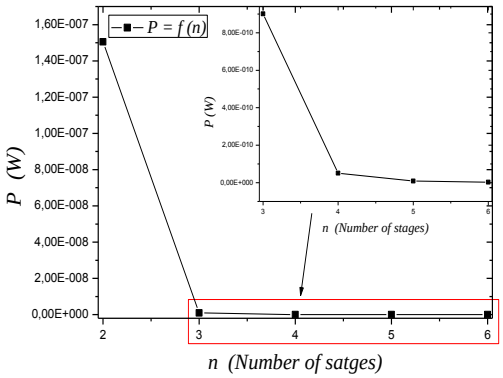

Figure 7 Power as a function of n for MSCM.

The simulation results show that the power consumption for Multi-Stage mirror of *n* stage is ultra low in order of hundreds nW, this proves that this topology has the lowest power consumption compared to the mirrors proposed in literary research [23-24-25].

Theoretically the decrease in output current I_{OUT} is leading to the lifting of the output resistance value according to (Equation 14). The simulation results showed that the output resistance of our mirror is increased as the *n* number of stages increases as shown in Figure 8. This is consistent with the theoretical principles.

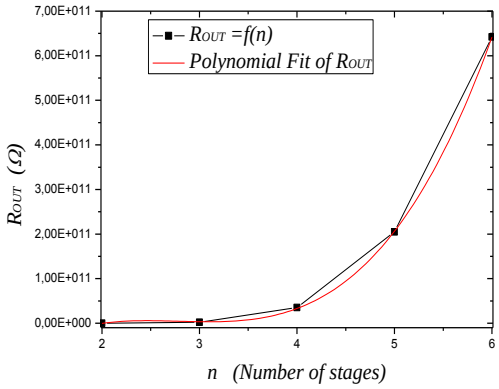

Figure 8 Rout as a function of n for MSCM.

In saturation region, V_{DD}=1.2V and at room temperature, R_{OUT} output resistance curve in Figure 8 can be fitted to the following equation:

$$R_{OUT} = (0.197\ n^3 - 1.64\ n^2 + 4.516\ n - 4.036) * 10^{11} \quad (16)$$

This rise in R_{OUT} output resistance leads to the high performance of our current mirror, and this is what is needed in the field of scientific research. The second section of our work, showed that the properties of the current mirror are improved by increasing the number of proposed mirror stages, which ultra low power consumption and ultra high output resistance with the current ratio is equal 1, i.e. this ratio is independent of the increase of *n* number of stages. The MSCM circuit retains on current mirroring accuracy whatever the increase in value of *n*.

4. CONCLUSION

The current mirrors have been designed using 130nm CMOS(6H-SiC) technology, then simulated these CMs under PSpice BSIM3v3 software in this. From the different characteristics of basic current mirrors in this technology, we have shown that these mirrors are operating correctly and characterized by better properties in a temperature range of – 200°C to 700°C, at supply voltage 1.2V. The comparison between the basic CMs showed that the Multi-Stage mirror is characterized by better properties. This is what motivated us to study the Multi-Stage mirror to prove that the performance of this mirror improves as

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the increase number of stages. Current mirrors on 130nm CMOS(6H-SiC) technology have the advantage of use in hostile and severe environments with low voltage and low power consumption.

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